Please add the following new claims:

-- 10. The semiconductor wafer according to claim 1, wherein the markings include alphanumeric characters. --

-- 11. The semiconductor wafer according to claim 10, wherein the alphanumeric characters are arranged in a pattern of 5 dot marks by 9 dot marks. --

-- 12. The semiconductor wafer according to claim 1, wherein the markings are arranged on the inner surface of the notch prior to fabrication steps of a slicing step, and before mirror face fabrication step and chemical polishing step. --

-- 13. The semiconductor wafer according to claim 1, wherein the markings contain all the history information concerning fabrication steps for fabricating the semiconductor wafer. --

REMARKS

In the foregoing amendments, claim 1 was amended to further define that the markings have history information concerning fabrication steps for fabricating the semiconductor wafer, which markings can be read after the semiconductor wafer is fabricated. New claims 10 and 11 define that the

markings include alphanumeric characters, which are arranged in a pattern of 5 x 9 of the dot marks. New claims 12 and 13 define that the markings are arranged on the inner surface of the notch prior to fabrication steps of a slicing step, and before mirror face fabrication step and chemical polishing step, or that the markings contain all the history information concerning fabrication steps for fabricating the semiconductor wafer. These aspects of applicant's claimed invention are described in the present specification disclosure on pages 19-21 and 24. Accordingly, claims 1-13 are in the application for consideration by the examiner.

Attached hereto is a marked-up version of the changes made to claims 1, 5, 8 and 9 by the current amendment. The attached pages are captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**."

The Official action mailed February 21, 2002, set forth three different prior art rejections of the claims. The first two were rejections of Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over either U.S. Patent No. 4,418, 467 of Iwai or U.S. Patent No. 6,268,641 of Yano. The third rejection was a rejection of Claims 2-9 under 35 U.S.C. § 103(a) over Yano in further view of U.S. Patent No. 6,004,405 of Oishi *et al.* (Oishi). In these rejections, it was acknowledged that the teachings of the cited references do not teach a dot mark having a maximum length of 1 to 13 μm on an inner wall surface of a notch formed on an outer peripheral face of the semiconductor wafer. However, the position was taken that it would have been an obvious matter of

design choice to change the dot mark to have a maximum length of 1 to 13 microns on an inner face wall of a notch formed on an outer peripheral face of the semiconductor wafer, because such a modification would have involved a mere change in the size of a component.

Applicant respectfully submits that the teachings of Iwai, Yano and/or Oishi either taken alone or in combination do not contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103.

The differences between these teachings and the presently claimed invention were set forth in applicant's response filed on July 22, 2002, which comments are incorporated herein by reference. In summary, the teachings of Iwai, Yano and Oishi propose markings on semiconductor wafers. Iwai proposes placing the marks on the circumferential edge of the wafer. The teachings of Yano proposes identification indication formed on the slant face extending from the peripheral portion of the side surface of the wafer. The teachings of Yano also apparently proposes identification formed on the peripheral portion of the semiconductor wafer, which is then covered with the cover member during processing. Oishi proposes marks carved on the chamfered edge of the wafer. None of these teachings contemplate or suggest a semiconductor wafer having a notch formed on an outer peripheral face thereof, an *inner wall face of the notch* containing markings with *history information* concerning fabrication steps for fabricating the semiconductor

wafer, which *markings can be read after the semiconductor wafer is fabricated,* and the markings are made from dot marks respectively having a maximum length of 1 to 13 μm, as presently claimed.

In the presently claimed invention, the dot marks have a maximum length of 1 to 13 μm. The size of the dot marks and their location on an inner face wall of a notch formed on a outer peripheral of the face of the semiconductor wafer enables the use of alphanumeric characters to mark individual semiconductor wafers for the purposes of identifying the wafers. The prior art was unable to mark the wafers individually and generally relied upon batch numbering. Furthermore, the markings on the presently claimed the semiconductor wafer can be read after the semiconductor wafers fabricated, thereby providing a manner of identifying each individual semiconductor wafer, so that quality can be assured. The teachings of Iwai, Yano and/or Oishi do not remotely contemplate or suggest the structure or resulting function of applicant's claims.

Due to the size and location of the marks, as presently claimed, the influences of wafer processing, such as chemical mechanical polishing and chemical film deposition, which adversely affect the conventional IDs, can be minimized. This means that after wafer processing is completed, the markings in accordance with applicant's claimed invention can be easily read, whereas those of the conventional IDs cannot be read. The teachings of Iwai, Yano and/or Oishi do not remotely contemplate or suggest the size of the dot

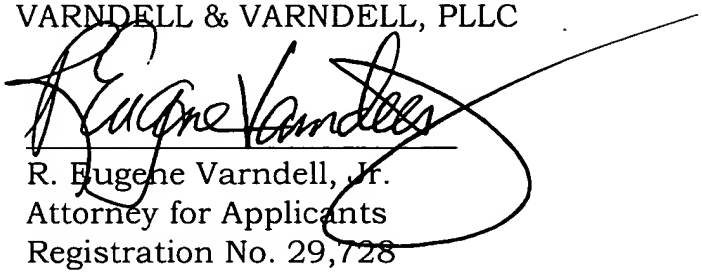
markings or the arrangement thereon as required in applicant's claimed invention. Therefore, applicant respectfully submits that the presently claimed invention is distinguishable from these teachings.

For the foregoing reasons, applicant respectfully submits that none of the teachings of Iwai, Yano and Oishi, either taken alone or in combination, contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the prior art rejections of applicant's claims in the outstanding Office action.

In view of the foregoing amendments and remarks, favorable consideration and allowance of claims 1-13 are respectfully requested. While it is believed that all the claims in this application are in condition for allowance, should the examiner have any comments or questions, it is respectfully requested that the undersigned be telephoned at the below-listed number to resolve any outstanding issues.

In the event that this paper is not timely filed, applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge the fee therefor, as well as any deficiency in the payment of the required fee(s) or credit any overpayment, to our Deposit Account No. 22-0256.

Respectfully submitted,
VARNDELL & VARNDELL, PLLC



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 5, 8 and 9 were amended as follows:

-- 1. (Twice amended) A semiconductor wafer having an outer peripheral face containing a notch, an inner wall face of the notch containing markings with history information concerning fabrication steps used to fabricate the semiconductor wafer, which markings can be read after fabrication of the semiconductor wafer is completed, and the markings being made from [a] dot [mark] marks respectively having a maximum length of 1 to 13 μm [on an inner wall face of a notch formed on an outer peripheral face thereof]. --

-- 5. (Twice amended) The semiconductor wafer according to Claim 2, wherein the dot [mark is] marks are formed on either one of the upper and lower inclined faces. --

-- 8. (Amended) The semiconductor wafer according to Claim 1, wherein the dot [mark is] marks are formed by irradiating a laser beam. --

-- 9. (Twice amended) The semiconductor wafer according to Claim 1, wherein the dot [mark has] marks have a height in the range of 0.005 to 5 μm. --